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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/711,501	09/22/2004	Glenn G. Daves	FIS920040002US1	5500

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LAW OFFICE OF DELIO & PETERSON, LLC.
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EXAMINER	
ABOAGYE, MICHAEL	
ART UNIT	PAPER NUMBER
1793	
MAIL DATE	DELIVERY MODE
05/01/2008	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary	Application No.	Applicant(s)	
	10/711,501	DAVES ET AL.	
	Examiner	Art Unit	
	MICHAEL ABOAGYE	1793	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE *3* MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *17 January 2008*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-10 and 13-22* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *1-4 and 19-22* is/are allowed.

6)☒ Claim(s) *5-10* is/are rejected.

7)☒ Claim(s) *13-18* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 103

1. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

2. Claims 5 and 7-10 are rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view of Morganelli et al. (US Patent No. 7,047,633).

White discloses an electronic module and a method of making said module, the method comprising: attaching a chip (402, figure 4) to a substrate (404, figure 4) using a first solder interconnection array (406, figure 4); attaching an organic board (416, figure 6, and column 1, lines 6-15) to said substrate using a second solder interconnection array (412, figure 4) such that a space is defined between said board and said substrate; said second solder interconnection array residing entirely within said space (see, figure 4); and providing an underfill material within said space after said board has been attached to said substrate but prior to applying compressive forces to said electronic module (408, figure 4 and column 7, lines 24-46), Note the applicant in his own admission as per figure 1 and paragraph 8, that it is common practice to apply

compressive force to the assembly after attaching the board to the substrate. White teaches providing a mechanical support structure comprising at least one rigid metallic ball within said space (column 5, lines 42-47) and providing a mechanical support structure comprising a frame (916, figure 9) within said space (White see, column 8, lines 25-28). White teaches a ceramic substrate and an organic board (column 5, lines 30-35) an that since the CTE value is a material property, Said a ceramic substrate and an organic board similarly a ceramic substrate has a CTE below Tg of about 18 ppm/°C to about 21 ppm/°C and said organic substrate has a CTE below Tg of about 12 ppm/°C to about 25 ppm/°C. White also teaches dual melt solder interconnect (White, column 2, lines 35-52 and column 5, lines 48-60).

White does not expressly teach an underfill material partially encapsulating said second solder interconnection array at discrete locations.

However, Morganelli et al., teaches a method of forming an electronic module using solder interconnect and applying underfill to partially encapsulate a fraction of the space or gap between the solder interconnect, thereby providing a space or room for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the process of White to use partial underfill technique as taught by Morganelli et al. to provide space or room for volatile compounds to escape from the package during a reflow process (Morganelli et al., column1, lines 10-30, and column 8, lines 15-20).

3. Claim 6 is rejected under 35 U.S.C. 103(a) as being unpatentable over White (US Patent No. 5,535,526) in view Morganelli et al. (US Patent No. 7,047,633) as applied to claim 5 above and further in view of Baba et al. (US Patent No. 6,582,993).

White, and Morganelli et al. do not expressly teach cleaning the organic board or substrate prior to depositing the underfill.

Baba et al. teaches cleaning the organic board or substrate prior to depositing the underfill to improve the wetness of the underfill receiving area (Baba et al., column 4, lines 31-40).

It would have been obvious to one of ordinary skill in the art at the time the applicant's invention was made to modify the combined invention of White and Morganelli et al to clean the organic board or substrate prior to depositing the underfill as taught by Baba et al. to improve the wetness of the underfill receiving region (Baba et al., column 4, lines 31-40)

Allowable Subject Matter

4. Claims 1-4 and 19-22 are allowed.

Claims 13-18 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

The following is a statement of reasons for the indication of allowable subject matter: The prior art fail to teach solder interconnection array such that a space is defined between said board and said substrate having a gap height ranging from about 300 microns to about 900 microns, with other claimed features.

Response to Arguments

5. The examiner acknowledges the applicants' amendment received by USPTO on January 17, 2008. Claims 1-10 and 13-22 remain under consideration in the application.

6. Applicant's arguments with respect to claims 5-10 have been fully considered but they are not persuasive. Applicant argues that nowhere in the White reference is it disclosed, contemplated or suggested to form electronic modules by attaching a chip to a first surface of a substrate using a first solder interconnection array and attaching a board to a second surface of the substrate using a second solder interconnection array to define a space there-between the board and substrate, which is underfilled after the board has been attached to the substrate but prior to applying compressive forces to the

electronic module, as is currently claimed. The examiner disagrees. Applicant's attention is drawn to figure 1 of White in which a flow chart of the process step is illustrated. Said flow chart of figure 1 distinctly shows the attaching or connection step before the injection of the underfill or the encapsulant. The Applicant argues that Morganelli does not disclose, contemplate or suggest that an electronic module is formed by attaching chip to a first surface of a substrate using a first solder interconnection array and attaching a board to a second surface of the substrate using a second solder interconnection array to define a space there-between that is underfilled after the board has been attached to the substrate but prior to applying compressive forces to the electronic module. The examiner agrees in part that Morganelli et al. does not teach a first and second level assembly as claimed, however, Morganelli et al. teaches attaching a component to a substrate and injecting an underfill material in the space therebetween. It is noted that most of applicant's argument against Morganelli et al. or Baba et al. references are not pertinent to the examiner's position and/ or assertions made in the prior office action. The applicant argues about limitations already met by the White. It should be noted that Morganelli et al. reference is cited for the limitation of providing a partial underfill material in an interconnection to remedy the deficiency in the teaching of White. Baba et al. reference is also only cited for the limitation of providing a cleaning step.

Conclusion

7. Applicant's amendment necessitated the new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

8. Any inquiry concerning this communication or earlier communications from the examiner should be directed to MICHAEL ABOAGYE whose telephone number is (571)272-8165. The examiner can normally be reached on Mon - Fri 8:30am - 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Roy King can be reached on 571-272-1244. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

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Assistant Examiner,
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